Sheng-Jung Yu

(510) 289-6940 | shengjungyu@berkeley.edu

Research Interests

Design Automation for Cyber-Physical Systems and Integrated Circuit Systems, Design Methodologies including Platform-based Design and Contract-based Design

Education

University of California, Berkeley — *Berkeley, CA*

Ph.D. student in Electrical Engineering and Computer Sciences — *08/2020 - Present*

- Cumulative GPA: **3.89**/4.00.
- Advisor: Alberto Sangiovanni-Vincentelli

National Taiwan University (NTU) — *Taipei, Taiwan*

B.S. in Electrical Engineering — *09/2015 - 06/2019*

- Cumulative GPA: **4.28**/4.30. (**1st**/190)

Work Experience

Cadence Design System Inc. — *San Jose, CA*

Software Engineering Intern — *5/2023 - 8/2023*

- Applied Bayesian optimization to optimize automatic layout generation algorithm configuration for analog circuits.
- Transferred Tree-Parzen Estimator (TPE) to modified circuits and achieved an over 40% reduction in required iterations.

Portwell Inc. — *Shulin, New Taipei City*

R&D Intern — *7/2018 - 9/2018*

- Implemented the Harris corner detection algorithm in OpenCL.
- Deployed the camera with the FPGA to achieve real-time corner detection.

Honors & Awards

2023	**Graduate Division Conference Travel Grant**, Graduate Division, UC Berkeley
2020	**A. Richard Newton Young Student Fellow**, the 57th Design Automation Conference
2020 - 2024	**Berkeley Fellowship for Graduate Study**, Graduate Division, UC Berkeley
2020	**Best Paper Award**, the 25th Asia and South Pacific Design Automation Conference
2016-2019	**Dean's List, 8 times**, National Taiwan University
2018	**2nd place**, CAD Contest, Ministry of Education, Taiwan

Research Experience

Graduate Student Researcher, **iCyPhy, Prof. Alberto Sangiovanni-Vincentelli** — *Berkeley, CA*

Design Automation of Cyber-physical Systems with Contract-based Design — *8/2020 - present*

- Proposed and implemented a iterative optimization tool that combines contract-based design with black-box optimization techniques such as Bayesian optimization.

Contracts for Physical Systems — *11/2022 - present*

- Proposed constraint-behavior contracts, a new contract formalism for specifying physical systems.
- Eliminated the need to consider port directions and solve implicit equations for specification.

Theory and Tools for Automation of Design in Assume-Guarantee Contracts — *1/2021 - present*

- Identified the vacuous implementation problem in assume-guarantee contracts which cause independently developed subcomponents not able to be integrated into the system.
- Formulated the strong replaceability as the requirements to prevent the vacuous implementation problem.

Undergraduate Research Assistant, **Electronic Design Automation Lab, Prof. Yao-Wen Chang** — *Taipei, Taiwan*

Optical Network-on-Chip (ONoCs) Design Automation. — *12/2018 - 11/2019*

- Devised and implemented the first fully automated topological structure and physical layout codesign engine for Wavelength-Routed Optical Networks-on-Chip.
- Outperformed the state-of-the-art WRONoC design flow by a 25% reduction in the maximum insertion loss.

Optical Interconnect Routing — *12/2017 - 11/2018*

- Proposed and implemented a WDM-aware clustering algorithm to minimize both insertion loss and wire length.
- Outperformed the state-of-the-art algorithm by a 60% insertion loss reduction, a 45% wire length reduction, an 86% wavelength power reduction and an 1.9X speedup.

***Undergraduate Research Assistant*, Digital Circuits and Systems Lab, Prof. Chia-Hsiang Yang** *Taipei, Taiwan*

Digital Accelerator IC design *04/2018 - 11/2019*

- Designed an accelerator for IoT communications based on Double Ratchet Algorithm, an end-to-end communication protocol.
- Taped out the chip in June 2020. The chip occupies only 34% area, and consumes only 46% energy for each operation, compared with the previous work in ISSCC.

***Undergraduate Research Assistant*, Iris Lab, Prof. Iris Hui-Ru Jiang** *Taipei, Taiwan*

Timing-Aware Fill Insertion *07/2018 - 04/2019*

- Designed and Implemented an equivalent capacitance guided dummy fill insertion engine for 2018 ICCAD contest.
- Outperformed the state-of-the-art work by over 27% and the paper won the best paper award in *ASPDAC-20*.

Relevent Courses

Mathematics	Convex Optimization and Approximation, Introduction to Abstract Algebra Linear Algebra, Discrete Mathematics, Probabilities and Statistics.
Hardware System	Computer-aided VLSI System Design, Digital Signal Processing in VLSI Design, Integrated Circuit Design, Introduction to Embedded Systems, Computer Architecture and Engineering.
Design Automation	Physical Design for Nanometer ICs, Logic Synthesis and Verification, Formal Methods: Specification, Verification, and Synthesis , Numerical Simulation and Modeling, Embedded System Design: Modeling, Analysis, and Synthesis, Introduction to Electronic Design Automation
Computer Science	Machine Learning, The Design and Analysis of Algorithm, Data Structure and Programming

Skills

Natural Languages	Mandarin (Native), Taiwanese (Native), English (Proficient), Japanese (Intermediate, JLPT N3)
Programming Languages	C/C++, Python, LaTeX, Matlab, Verilog
EDA tools	nWave, ncverilog, Design Compiler, Innovus, SPICE

Publications

Conference Paper:

[C1] **Sheng-Jung Yu**, Chen-Chien Kao, Chia-Han Huang, and Iris Hui-Ru Jiang, "Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability," in *Proceedings of the 25th Asia and South Pacific Design Automation Conference (ASPDAC-20)*. **(Best Paper Award)**

[C2] Yu-Sheng Lu, **Sheng-Jung Yu**, and Yao-Wen Chang, "A Provably Good Wavelength-Division-Multiplexing-Aware Clustering Algorithm for On-Chip Optical Routing," in *Proceedings of Design Automation Conference (DAC-20)*.

[C3] Yu-Sheng Lu, **Sheng-Jung Yu**, and Yao-Wen Chang, "Topological Structure and Physical Layout Codesign for Wavelength-Routed Optical Networks-on-Chip," in *Proceedings of Design Automation Conference (DAC-20)*.

[C4] **Sheng-Jung Yu**, Yu-Chi Lee, and Chia-Hsiang Yang, "A 1.18mW Double Ratchet Cryptographic Processor with Backward Secrecy for IoT Devices," in *IEEE Asian Solid-State Circuit Conference (A-SSCC-21)*.

[C5] **Sheng-Jung Yu**, Inigo Incer, and Alberto Sangiovanni-Vincentelli, "Constraint-Behavior Contracts: A Formalism for Specifying Physical Systems," in *Proceedings of 21st ACM-IEEE International Symposium on Formal Methods and Models for System Design (MEMOCODE-23)*.

[C6] **Sheng-Jung Yu**, Inigo Incer, and Alberto Sangiovanni-Vincentelli, "Contract Replaceability for Ensuring Independent Design using Assume-Guarantee Contracts ," in *Proceedings of 21st ACM-IEEE International Symposium on Formal Methods and Models for System Design (MEMOCODE-23)*.

Journal Paper:

[J1] Yu-Sheng Lu, Yan-Lin Chen, **Sheng-Jung Yu**, and Yao-Wen Chang, "Topological Structure and Physical Layout Co-design for Wavelength-Routed Optical Networks-on-Chip," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 7, pp. 2237–2249, July 2022.

[J2] Yu-Sheng Lu, **Sheng-Jung Yu**, and Yao-Wen Chang, "On-Chip Optical Routing with Provably Good Algorithms for Path Clustering and Assignment," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 11, pp. 4653–4666, Nov 2022.

[J3] **Sheng-Jung Yu**, Yu-Chi Lee, Liang-Hsin Lin, and Chia-Hsiang Yang, "An Energy-Efficient Double Ratchet Cryptographic Processor With Backward Secrecy for IoT Devices," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 6, pp. 1810–1819, June 2023.

[J4] Shaokai Lin, Yatin A. Manerkar, Marten Lohstroh, Elizabeth Polgreen, **Sheng-Jung Yu**, Chadlia Jerad, Edward A. Lee, and Sanjit A. Seshia, "Towards Building Verifiable CPS using Lingua Franca," in *ACM Transactions on Embedded Computing Systems*, vol. 22, no. 5s, pp. 1–24, Sept 2023.