Sheng-Jung Yu

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Research Interests

Electronic Design Automation (Physical Design, Design for Manufacturability), Integrated Circuit Systems

Education

University of California, Berkeley (UC Berkeley) *Berkeley, CA*

Ph.D. in Electrical Engineering and Computer Sciences *08/2020 - Present*

National Taiwan University (NTU) *Taipei, Taiwan*

B.S. in Electrical Engineering *09/2015 - 06/2019*

- Cumulative GPA: **4.28**/4.30. (**1st**/190)

Honors & Awards

2020	**A. Richard Newton Young Student Fellow**, the 57th Design Automation Conference
2020	**Berkeley Fellowship for Graduate Study**, Graduate Division, UC Berkeley
2020	**Best Paper Award**, the 25th Asia and South Pacific Design Automation Conference
2016-2019	**Dean's List, 8 times**, National Taiwan University
2018	**4th place**, 2018 CAD Contest at ICCAD
2018	**2nd place**, CAD Contest, Ministry of Education, Taiwan

Research Experience

***Undergraduate Research Assistant*, Electronic Design Automation Lab, Prof. Yao-Wen Chang** *Taipei, Taiwan*

Optical Network-on-Chip (ONoCs) Design Automation. *12/2018 - 11/2019*

- Devised and implemented the first fully automated topological structure and physical layout codesign engine for Wavelength-Routed Optical Networks-on-Chip.
- Outperformed the state-of-the-art WRONoC design flow by a 25% reduction in the maximum insertion loss.

Optical Interconnect Routing *12/2017 - 11/2018*

- Proposed and implemented a WDM-aware clustering algorithm to minimize both insertion loss and wire length.
- Outperformed the state-of-the-art algorithm by a 60% insertion loss reduction, a 45% wire length reduction, an 86% wavelength power reduction and an 1.9X speedup.

***Undergraduate Research Assistant*, Digital Circuits and Systems Lab, Prof. Chia-Hsiang Yang** *Taipei, Taiwan*

Encryption IC design *04/2018 - 11/2019*

- Designed an accelerator for the end-to-end encryption Signal Protocol.
- Integrated cryptographic primitives including SHA-256, Elliptic Curve 25519 and AES-256.

***Undergraduate Research Assistant*, Iris Lab, Prof. Iris Hui-Ru Jiang** *Taipei, Taiwan*

Timing-Aware Fill Insertion *07/2018 - 04/2019*

- Designed and Implemented an equivalent capacitance guided dummy fill insertion engine for 2018 ICCAD contest.
- Outperformed the state-of-the-art work by over 27% and the paper won the best paper award in *ASPDAC-20*.

Publications

1. **Sheng-Jung Yu**, Chen-Chien Kao, Chia-Han Huang and Iris Hui-Ru Jiang, "Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability," in *Proceedings of the 25th Asia and South Pacific Design Automation Conference (ASPDAC-20)* **(Best Paper Award)**
2. Yu-Sheng Lu, **Sheng-Jung Yu** and Yao-Wen Chang, "A Provably Good Wavelength-Division-Multiplexing-Aware Clustering Algorithm for On-Chip Optical Routing," in *Proceedings of Design Automation Conference (DAC-20)*,
3. Yu-Sheng Lu, **Sheng-Jung Yu** and Yao-Wen Chang, "Topological Structure and Physical Layout Codesign for Wavelength-Routed Optical Networks-on-Chip," in *Proceedings of Design Automation Conference (DAC-20)*,

Teaching Experience

***Teaching Assistant*, Electrical Engineering Lab (Digital Circuit), Prof. Chia-Hsiang Yang** *09/2018-01/2019*

- Undergraduate-level lab course about hardware systems.
- Instructed 30 students in 10 groups about random number generator.

Skills

Natural Languages	Mandarin (Native), Taiwanese (Native), English (Proficient), Japanese (Intermediate, JLPT N3)
Programming Languages	C/C++, Python, LaTeX, Matlab, Verilog
EDA tools	nWave, ncverilog, Design Compiler, Innovus, SPICE